CLAIMS

1. An electrically erasable and programmable memory, comprising:

memory cells;

a verify-program device arranged for saving a datum in one of the memory cells by repeating a verify-program cycle until the datum is saved in the memory cell, without exceeding N cycles, the verify-program cycle including reading the memory cell then applying a pulse of a programming voltage to the memory cell if the datum to be saved has a program logic value and if the datum read in the memory cell has an erase logic value;

an erase verify device arranged for:

supplying an erase verify signal having a determined value when the datum read in a memory cell during the first verify-program cycle of an operation of programming the memory cell, has an erase logic value; and

atching the erase verify signal before applying the first pulse of programming voltage to the memory cell.

2. The memory according to claim 1 wherein the erase verify device is arranged for supplying an erase verify signal having said determined value when a datum to be saved itself has an erase logic value.

3. The memory according to claim 1, comprising a determined number of sense amplifiers for simultaneously reading a corresponding number of selected memory cells during an operation of saving data in the selected memory cells, and wherein the erase verify device comprises a corresponding number of erase verify circuits, each erase verify circuit being linked to a respective one of the sense amplifiers and supplying an individual signal for erase verifying a memory cell having said determined value when the datum read in the memory cell during the first verify-program cycle of the memory cell has the erase logic value.

4. The memory according to claim 3 wherein an erase verify circuit comprises a logic gate receiving at one input the datum read during the first verify-program cycle of the memory cell, and supplying the individual erase verify signal.

5. The memory according to claim 4 wherein the logic gate is arranged for combining the datum read in the memory cell during the first verify-program cycle of the memory cell and the datum to be saved in the memory cell, the individual erase verify signal varying according to the result of the combination.

6. The memory according to claim 5 wherein the logic gate is of OR or NOR type.

7. The memory according to claim 3 wherein the erase verify device comprises a logic circuit for collecting all the individual erase verify signals supplied by the erase verify circuits, and for supplying a collective signal for erase verifying a plurality of memory cells.

8. The memory according to claim 7, comprising means for latching the value of the collective verify signal before applying the first pulse of programming voltage.

9. The memory according to claim 8, comprising means for supplying a series of pulses of verify signals applied to the verify-program device, and for supplying an erase verify latching signal after sending the first pulse of the verify signal.

10. A method for testing an electrically erasable and programmable memorythat includes memory cells and a verify-program device, the method comprising

saving a datum in one of the memory cells by repeating a verify-program cycle until the datum is saved, without exceeding N cycles, the verify-program cycle

comprising reading the memory cell that must receive the datum, then applying a pulse of a programming voltage to the memory cell if the datum to be saved in the memory cell has a program logic value and if the data read in the memory cell has an erase logic value;

supplying an erase verify signal having a determined value when the datum read in the memory cell during a first one of the verify-program cycles, has an erase logic value; and

latching the erase verify signal before applying the first pulse of programming voltage to the memory cell.

11. The method according to claim 10, further comprising supplying the erase verify signal having said determined value when the datum to be saved itself has the erase logic value.

12. The method according to claim 10, wherein the memory includes a determined number of sense amplifiers allowing a corresponding number of selected memory cells to be simultaneously read during an operation of saving data in the selected memory cells, the method comprising producing a number of individual erase verify signals during the saving of data corresponding to the corresponding number of selected memory cells.

13. The method according to claim 12, comprising combining the individual erase verify signals to supply a collective signal for erase verifying of the selected memory cells.

14. The method according to claim 13, comprising latching the collective erase verify signal before applying the pulse of programming voltageduring the first verify-program cycle.

15. An electrically erasable and programmable memory, comprising:

memory cells arranged in rows and a number of columns;

a first read circuit having an output and an input connected to a first one of the columns of memory cells and structured to read a datum stored in a selected one of the memory cells in the first column;

a first verify-program device having a first input connected to receive an input datum, a second input connected to the output of the first read circuit, and an output that supplies a program signal to program the datum into the selected memory cell;

a first erase verify device having a first input connected to receive the input datum, a second input connected to the output of the first read circuit, and an output that supplies an erase verify signal having a value that reflects whether the input datum is equal to the datum read by the first read circuit.

16. The memory according to claim 15 wherein the first erase verify device includes a logic gate of OR or NOR type having first and second inputs connected to the input datum and the output of the first read circuit, respectively.

17. The memory according to claim 15 wherein:

the first read circuit is one of a plurality of read circuits connected respectively to the columns, each read circuit being structured to read a datum stored in a selected one of the memory cells in the column to which the read circuit is connected;

the first verify-program device is one of a plurality of verify-program devices having outputs connected respectively to the columns, each verify-program device having a first input connected to an output of a corresponding one of the read circuits and a second input connected to receive a corresponding one of a plurality of input data; and

the first erase verify device is one of a plurality of erase verify devices, each erase verify device having a first input connected to the output of the

corresponding read circuit, a second input connected to receive the corresponding input data, and an output that supplies an individual erase verify signal having a value that reflects whether the corresponding input datum is equal to the datum read by the corresponding read circuit.

18. The memory according to claim 17, further comprising a logic circuit connected to receive the individual erase verify signals supplied by the erase verify circuits, and structured to supply a collective signal for erase verifying a plurality of memory cells.

19. The memory according to claim 18, further comprising a latch having an input connected to receive the collective verify signal.

20. The memory according to claim 19, further comprising a sequencer having a plurality of outputs connected to the read circuits, verify-program devices, and the latch, and being structured to cause the latch to latch the collective signal before the verify-program devices supply programming voltages to the memory cells in order to program the input data.